S-24CS01A/02A/04A H Series

105°C OPERATION 2-WIRE SERIAL E^{2}PROM FOR AUTOMOTIVE

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The S-24CS01A/02A/04A H series is a high temperature operation 2-wire serial E^{2}PROM for automotive components. The S-24CS01A/02A/04A H series has the capacity of 1 K-bit, 2 K-bit and 4 K-bit, and the organization is 128 words × 8 bits, 256 words × 8 bits and 512 words × 8 bits.
Page write and sequential read are available.

■ Features

- Low power consumption — Standby : 2.0 μA Max. (V_{CC} = 5.5 V)
  Read : 0.8 mA Max. (V_{CC} = 5.5 V)
- Operating voltage range — Read : 2.55 V to 5.5 V (at –40°C to +105°C)
  Write : 2.55 V to 5.5 V (at –40°C to +105°C)
- Page write : 8 bytes / page (S-24CS01A/02A)
  16 bytes / page (S-24CS04A)
- Sequential read
- Operating Frequency : 400 kHz (V_{CC} = 2.55 V to 5.5 V, at –40°C to +85°C)
  350 kHz (V_{CC} = 2.55 V to 5.5 V, at +85°C to +105°C)
- Write protect function during the low power supply voltage
- Endurance: 10^6 cycles/word*1 (at +85°C)
  5×10^5 cycles/word*1 (at +105°C)
- Data retention: 100 years (at +25°C)
  20 years (at +105°C)
- S-24CS01A : 1 Kbit
- S-24CS02A : 2 Kbit
- S-24CS04A : 4 Kbit
- Write protect : 100%
- Lead-free, Sn 100%, halogen-free*2

***1.** For each address (Word: 8-bit)
***2.** Refer to "■ **Product Name Structure**" for details.

■ Packages

- 8-Pin SOP(JEDEC)
- 8-Pin TSSOP
- TMSOP-8

Caution **Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.**

■ Pin Configurations

8-Pin SOP(JEDEC)
Top view

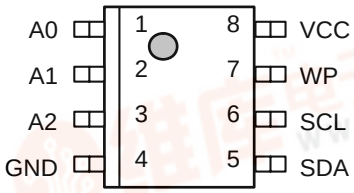


Figure 1

S-24CS01AFJ-TBH-U
S-24CS02AFJ-TBH-U
S-24CS04AFJ-TBH-U

Table 1

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*1)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protect input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

8-Pin TSSOP
Top view

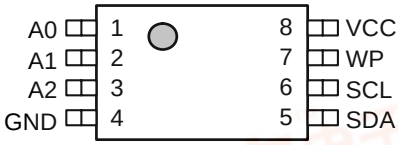


Figure 2

S-24CS01AFT-TBH-U
S-24CS02AFT-TBH-U
S-24CS04AFT-TBH-U

Table 2

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*1)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protect input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

TMSOP-8
Top view

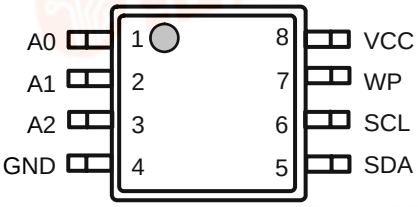


Figure 3

S-24CS01AFM-TFH-U
S-24CS02AFM-TFH-U
S-24CS04AFM-TFH-U

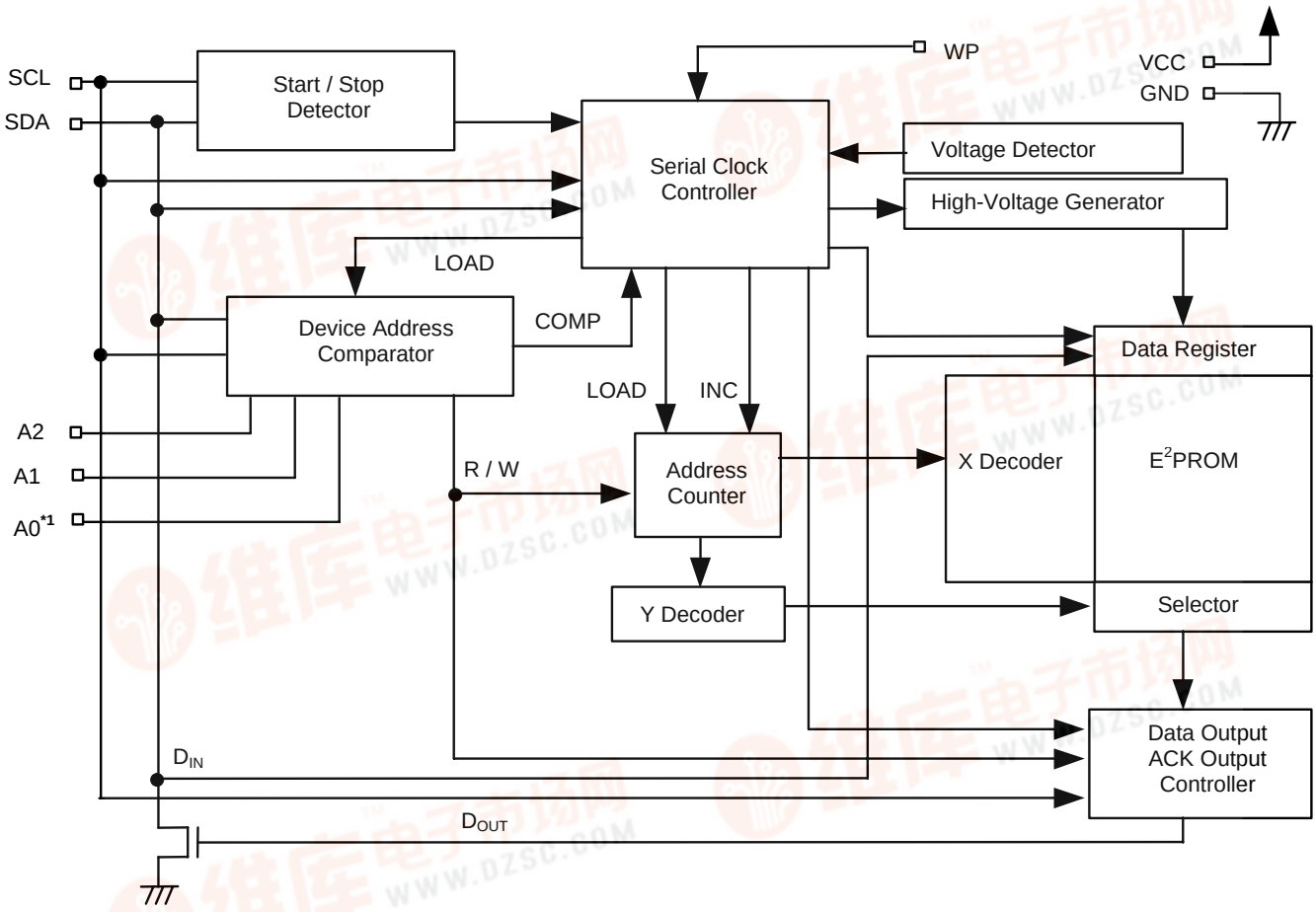
Table 3

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*1)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protect input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

Remark 1. See Dimensions for details of the package drawings.
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Block diagram



***1.** This pin is not available for S-24CS04A.

Figure 4

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to +7.0	V
Output voltage	V_{OUT}	−0.3 to +7.0	V
Operating ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Recommended Operating Conditions

Table 5

Item	Symbol	Conditions	−40°C to +85°C		+85°C to +105°C		Unit
			Min.	Max.	Min.	Max.	
Power supply voltage	V_{CC}	Read Operation	1.8	5.5	2.55	5.5	V
		Write Operation	2.55	5.5	2.55	5.5	V
High level input voltage	V_{IH}	V_{CC} = 4.5 V to 5.5 V	0.7×V_{CC}	V_{CC}	0.7×V_{CC}	V_{CC}	V
		V_{CC} = 2.55 V to 4.5 V	0.7×V_{CC}	V_{CC}	0.7×V_{CC}	V_{CC}	V
		V_{CC} = 1.8 V to 2.55 V	0.8×V_{CC}	V_{CC}	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V to 5.5 V	0.0	0.3×V_{CC}	0.0	0.3×V_{CC}	V
		V_{CC} = 2.55 V to 4.5 V	0.0	0.3×V_{CC}	0.0	0.3×V_{CC}	V
		V_{CC} = 1.8 V to 2.55 V	0.0	0.2×V_{CC}	—	—	V

■ Pin Capacitance

Table 6

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (S-24CS01A/02A: SCL, A0, A1, A2, WP)	—	10	pF
		V_{IN} = 0 V (S-24CS04A: SCL, A1, A2, WP)	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	—	10	pF

■ Endurance

Table 7

Item	Symbol	Operating ambient temperature	Min.	Max.	Unit
Endurance	N_W	−40°C to +85°C	10^6	—	cycles / word*1
		+85°C to +105°C	5×10^5	—	cycles / word*1

***1.** For each address (Word: 8 bits)

■ Data Retention

Table 8

Item	Symbol	Operating ambient temperature	Min.	Max.	Unit
Data retention	—	+25°C	100	—	year
		−40°C to +105°C	20	—	year

■ DC Electrical Characteristics

Table 9 (1/2)

Item	Symbol	Conditions	−40°C to +85°C						Unit
			V_{CC} = 4.5 V to 5.5 V f = 400 kHz		V_{CC} = 2.7 V to 4.5 V*1 f = 100 kHz		V_{CC} = 1.8 V to 2.7 V f = 100 kHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	—	—	0.8	—	0.3	—	0.2	mA
Current consumption (WRITE)	I_{CC2}	—	—	4.0	—	1.5	—	—	mA

***1.** V_{CC} = 2.55 V to 4.5 V in Write

Table 9 (2/2)

Item	Symbol	Conditions	+85°C to +105°C		Unit
			V_{CC} = 2.55 V to 5.5 V f = 350 kHz		
			Min.	Max.	
Current consumption (READ)	I_{CC1}	—	—	0.8	mA
Current consumption (WRITE)	I_{CC2}	—	—	4.0	mA

Table 10 (1/2)

Item	Symbol	Conditions	−40°C to +85°C						Unit
			V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.55 V to 4.5 V		V_{CC} = 1.8 V to 2.55 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	—	2.0	—	2.0	—	2.0	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	µA
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	—	0.4	—	—	V
		I_{OL} = 1.5 mA	—	0.3	—	0.3	—	0.5	V
Current address hold voltage	V_{AH}	—	1.5	5.5	1.5	4.5	1.5	2.55	V

Table 10 (2/2)

Item	Symbol	Conditions	+85°C to +105°C		Unit
			V_{CC} = 2.55 V to 5.5 V		
			Min.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	—	2.0	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	µA
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
		I_{OL} = 1.5 mA	—	0.3	V
Current address hold voltage	V_{AH}	—	1.5	5.5	V

■ AC Electrical Characteristics

Table 11 Measurement Conditions

Input pulse voltage	0.1×V_{CC} to 0.9×V_{CC}
Input pulse rising / falling time	20 ns
Output judgment voltage	0.5×V_{CC}
Output load	100 pF+ Pull-up resistor 1.0 kΩ

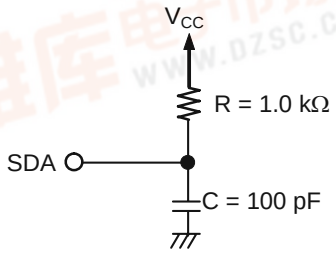


Figure 5 Output Load Circuit

Table 12

Item	Symbol	−40°C to +85°C						+85°C to +105°C		Unit
		V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.55 V to 4.5 V		V_{CC} = 1.8 V to 2.55 V		V_{CC} = 2.55 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	400	0	100	0	350	kHz
SCL clock time “L”	t_{LOW}	1.0	—	1.0	—	4.7	—	1.1	—	µs
SCL clock time “H”	t_{HIGH}	0.9	—	0.9	—	4.0	—	1.0	—	µs
SDA output delay time	t_{AA}	0.1	0.9	0.1	0.9	0.1	3.5	0.1	1.0	µs
SDA output hold time	t_{DH}	50	—	50	—	100	—	50	—	ns
Start condition setup time	$t_{SU.STA}$	0.6	—	0.6	—	4.7	—	0.6	—	µs
Start condition hold time	$t_{HD.STA}$	0.6	—	0.6	—	4.0	—	0.6	—	µs
Data input setup time	$t_{SU.DAT}$	100	—	100	—	200	—	100	—	ns
Data input hold time	$t_{HD.DAT}$	0	—	0	—	0	—	0	—	ns
Stop condition setup time	$t_{SU.STO}$	0.6	—	0.6	—	4.0	—	0.6	—	µs
SCL, SDA rising time	t_R	—	0.3	—	0.3	—	1.0	—	0.3	µs
SCL, SDA falling time	t_F	—	0.3	—	0.3	—	0.3	—	0.3	µs
Bus release time	t_{BUF}	1.3	—	1.3	—	4.7	—	1.3	—	µs
Noise suppression time	t_I	—	50	—	100	—	100	—	50	ns

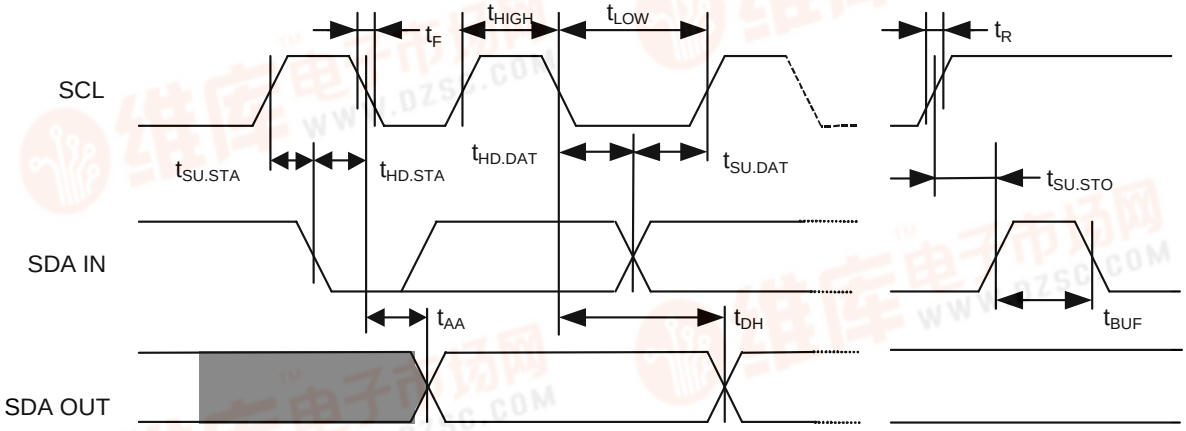


Figure 6 Bus Timing

Table 13

Item	Symbol	−40°C to +85°C V_{CC} = 2.55 V to 5.5 V			+85°C to +105°C V_{CC} = 2.55 V to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Write time	t_{WR}	—	4.0	10.0	—	4.0	10.0	ms

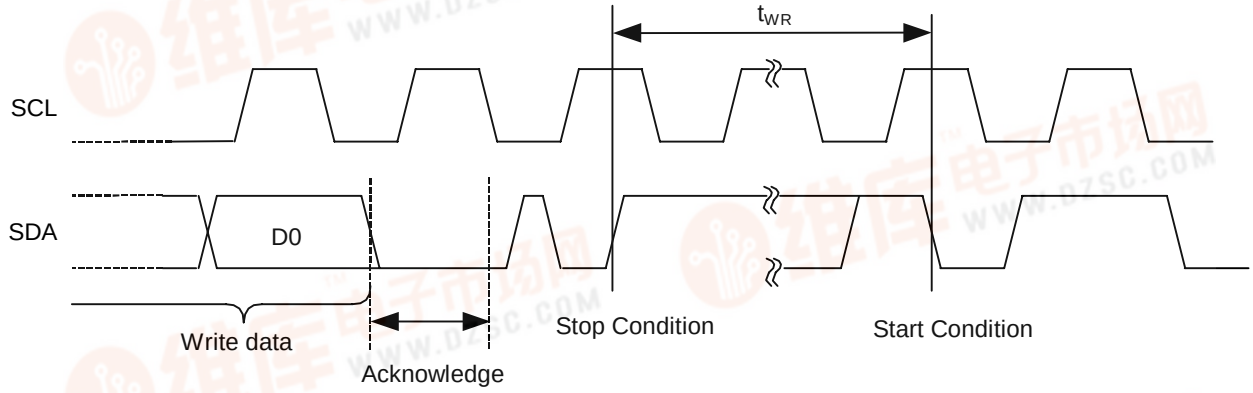


Figure 7 Write Cycle Timing

■ Pin Functions

1. Address input pins (A0, A1 and A2)

The slave address is assigned by connecting pins A0, A1 and A2 to the GND or to the V_{CC} respectively. One of the eight different slave address can be assigned to the S-24CS01A/02A by the combination of pins A0, A1 and A2.

The slave address is assigned by connecting pins A1 and A2 to the GND or to the V_{CC} respectively. One of the four different slave address can be assigned to the S-24CS04A by the combination of pins A1 and A2.

The given slave address, which is compared with the slave address transmitted from the master device, is used to select the one among the multiple devices connected to the bus. The address input pin should be connected to the GND or to the V_{CC}.

2. SDA (Serial data input / output) pin

The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
The SDA line is usually pulled up to the V_{CC}, and OR-wired with other open-drain or open-collector output devices.

3. SCL (Serial clock input) pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

4. WP (write protect input) pin

The write protect is enabled by connecting the WP pin to the V_{CC}. When there is no need for write protect, connect the pin to the GND.

■ Operation

1. Start condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the S-24CS01A/02A/04A initiates a write cycle.

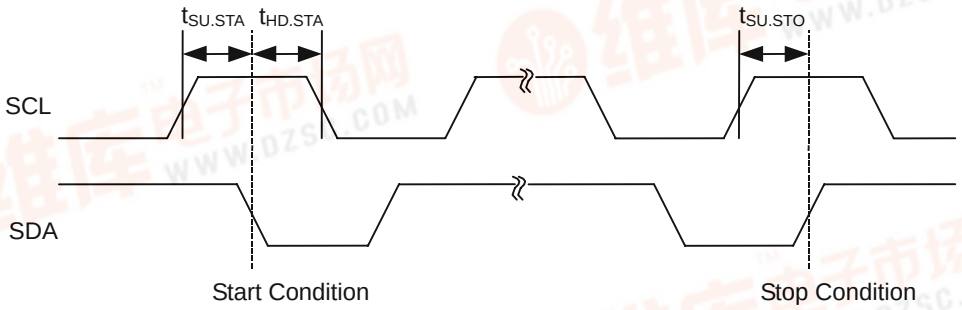


Figure 8 Start / Stop Conditions

3. Data transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

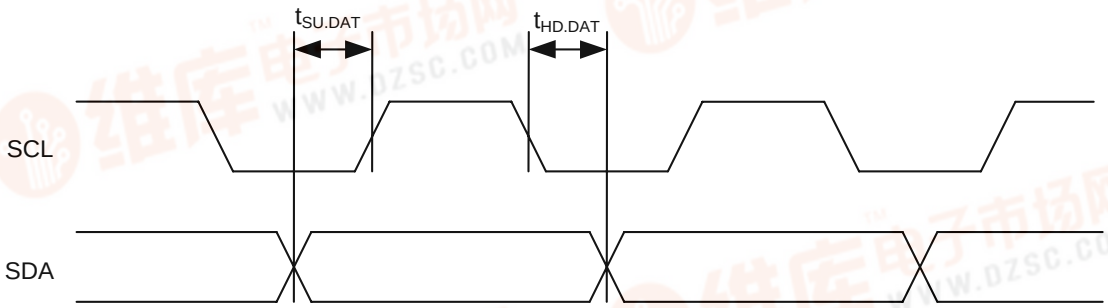


Figure 9 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

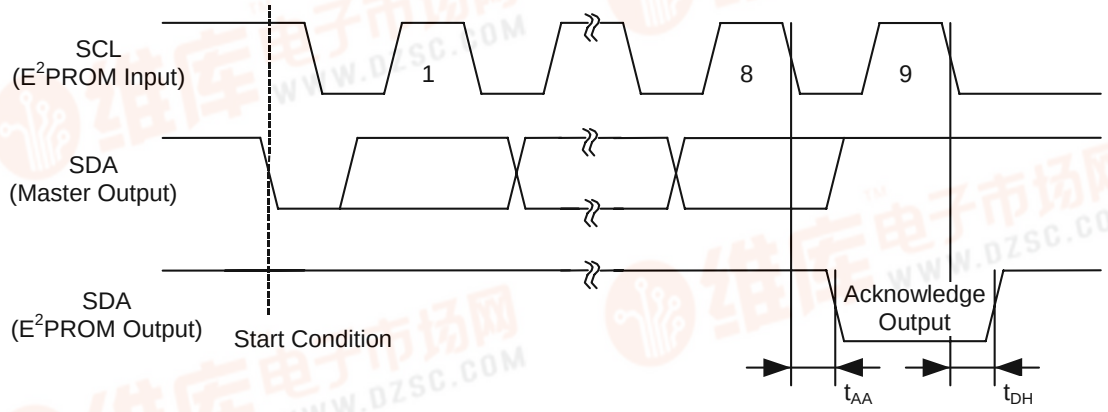


Figure 10 Acknowledge Output Timing

5. Device addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus.
The 4 most significant bits of the device address are called the "Device Code", and are fixed to "1010".

In S-24CS01A/02A, successive 3 bits are called the “Slave Address”. These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A0, A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.

In S-24CS04A, successive 2 bits are called the "Slave Address". These 2 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.
The successive 1 bit (P0) is used to define a page address and choose the two 256-byte memory blocks (Address 000h to 0FFh and 100h to 1FFh).

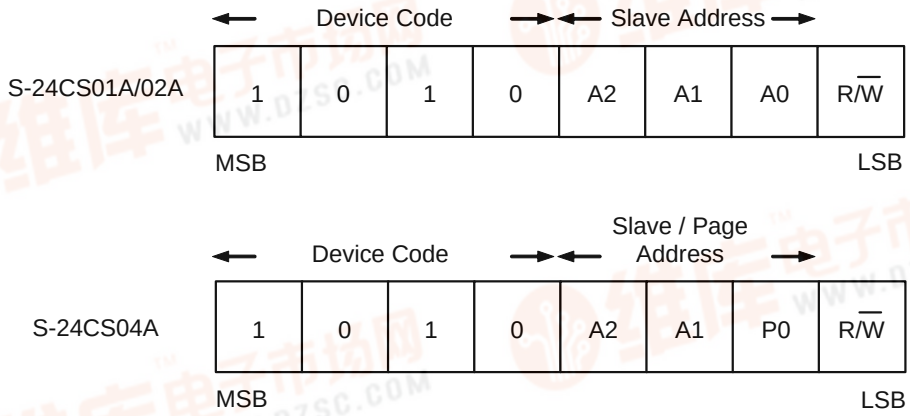
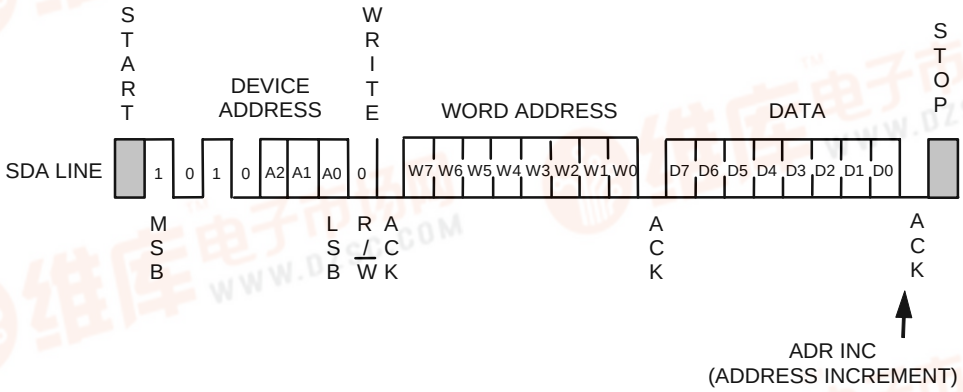


Figure 11 Device Address

6. Write

6. 1 Byte write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, the S-24CS01A/02A/04A acknowledges it. The S-24CS01A/02A/04A then receives an 8-bit word address and responds with an acknowledge. After the S-24CS01A/02A/04A receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

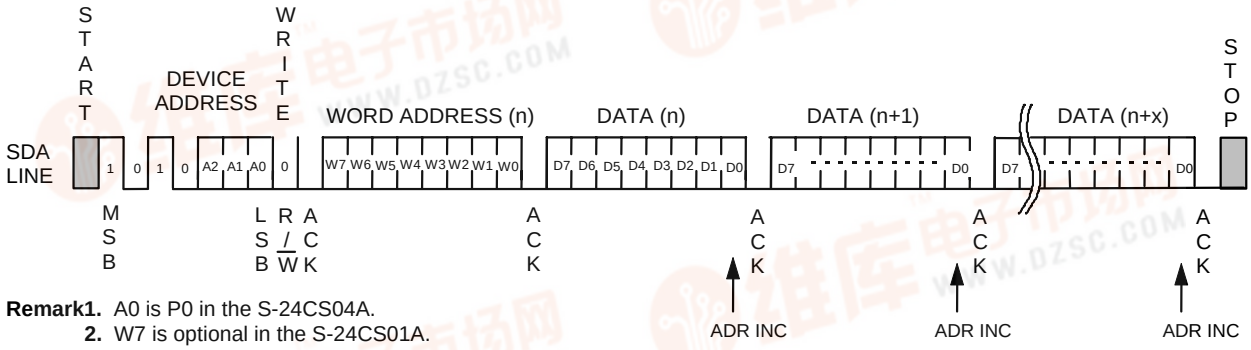


Remark 1. A0 is P0 in the S-24CS04A.
2. W7 is optional in the S-24CS01A.

Figure 12 Byte Write

6. 2 Page write

The page write mode allows up to 8 bytes to be written in a single write operation in the S-24CS01A/02A and 16 bytes to be written in a single write operation in the S-24CS04A.
Basic data transmission procedure is the same as that in the "Byte Write". But instead of generating a stop condition, the master transmits 8-bit write data up to 8 bytes before the page write.
When the S-24CS01A/02A/04A receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, it generates an acknowledge. Then the S-24CS01A/02A/04A receives an 8-bit word address, and responds with an acknowledge. After the S-24CS01A/02A/04A receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The S-24CS01A/02A/04A repeats reception of 8-bit write data and generation of acknowledge in succession. The S-24CS01A/02A/04A can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.



Remark1. A0 is P0 in the S-24CS04A.
2. W7 is optional in the S-24CS01A.

Figure 13 Page Write

In S-24CS01A/02A, the lower 3 bits of the word address are automatically incremented every time when the S-24CS01A/02A receives 8-bit write data. If the size of the write data exceeds 8 bytes, the upper 5 bits of the word address remain unchanged, and the lower 3 bits are rolled over and previously received data will be overwritten.

In S-24CS04A, the lower 4 bits of the word address are automatically incremented every time when the S-24CS04A receives 8-bit write data. If the size of the write data exceeds 16 bytes, the upper 4 bits of the word address and page address (P0) remain unchanged, and the lower 4 bits are rolled over and previously received data will be overwritten.

6. 3 Write protect

Write protect is available in the S-24CS01A/02A/04A. When the WP pin is connected to the V_{CC}, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND, the write protect is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.
There is no need for using write protect, the WP pin should be connected to the GND. The write protect is valid in the operating voltage range.

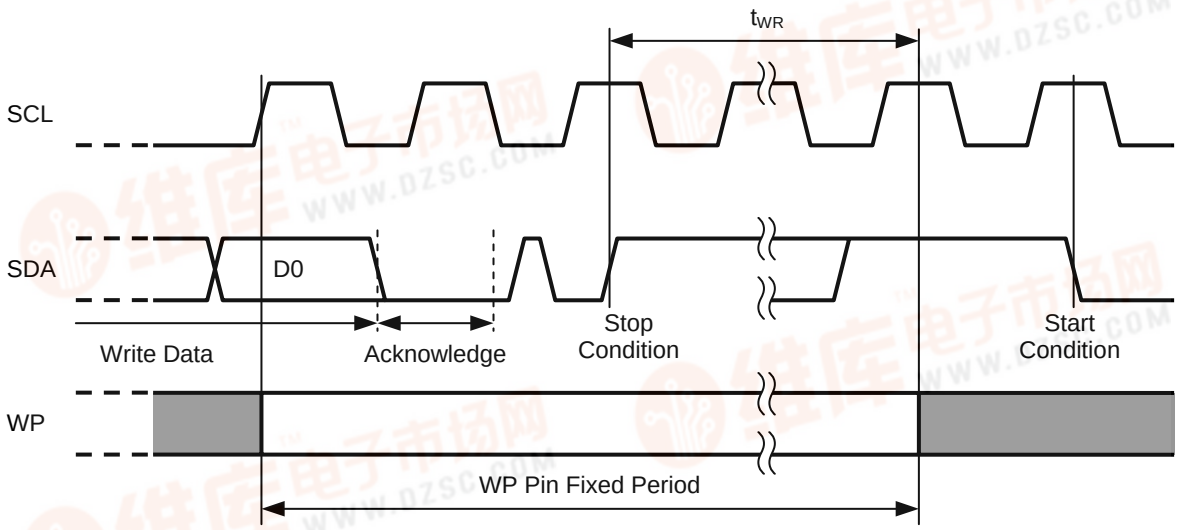


Figure 14 WP Pin Fixed Period

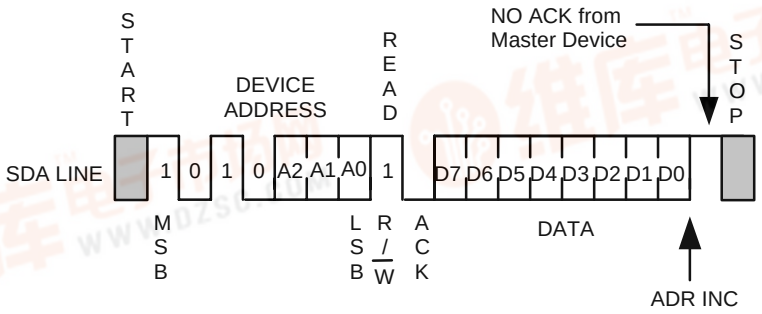
6. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in the S-24CS01A/02A/04A.
After the S-24CS01A/02A/04A receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the S-24CS01A/02A/04A by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the S-24CS01A/02A/04A, namely to the slave devices.
That is, if the S-24CS01A/02A/04A does not generate an acknowledge, the write cycle is in progress and if the S-24CS01A/02A/04A generates an acknowledge, the write cycle has been completed.
Keep the level of the WP pin fixed until acknowledge is confirmed.
It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

7. Read

7. 1 Current address read

Either in writing or in reading the S-24CS01A/02A/04A holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH}.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the S-24CS01A/02A/04A. This is called "Current Address Read".
In the following the address counter in the S-24CS01A/02A/04A is assumed to be “n”.
When the S-24CS01A/02A/04A receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition, it responds with an acknowledge. However, the page address (P0) in S-24CS04A becomes invalid and the memory address of the current address pointer becomes valid.
Next an 8-bit data at the address "n" is sent from the S-24CS01A/02A/04A synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.
The master device outputs stop condition not an acknowledge ,the reading of S-24CS01A/02A/04A is ended.



Remark A0 is P0 in S-24CS04A.

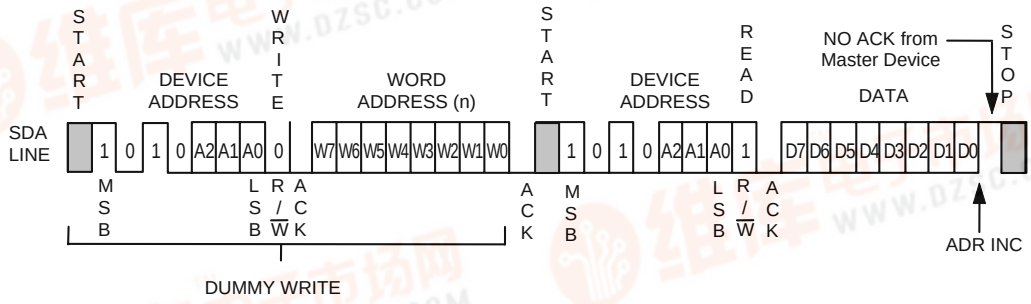
Figure 15 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the S-24CS01A/02A/04A.
In the read operation the memory address counter in the S-24CS01A/02A/04A is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper bits of the memory address (the upper bits of the word address and page address)*1 are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

***1.** S-24CS01A/02A is the upper 5 bits of the word address.
S-24CS04A is the upper 4 bits of the word address and the page address P0.

7. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the S-24CS01A/02A/04A receives a 7-bit device address and a 1-bit read / write instruction code set to "0" following a start condition, it responds with an acknowledge. The S-24CS01A/02A/04A then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the S-24CS01A/02A/04A by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the S-24CS01A/02A/04A receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the S-24CS01A/02A/04A in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge , the reading of S-24CS01A/02A/04A is ended.



Remark1. A0 is P0 in the S-24CS04A.
2. W7 is optional in the S-24CS01A.

Figure 16 Random Read

7. 3 Sequential read

When the S-24CS01A/02A/04A receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current and random read operations, it responds with an acknowledge.
An 8-bit data is then sent from the S-24CS01A/02A/04A synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the S-24CS01A/02A/04A incremented and makes it possible to read data in succession. This is called "Sequential Read".
The master device outputs stop condition not an acknowledge , the reading of S-24CS01A/02A/04A is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

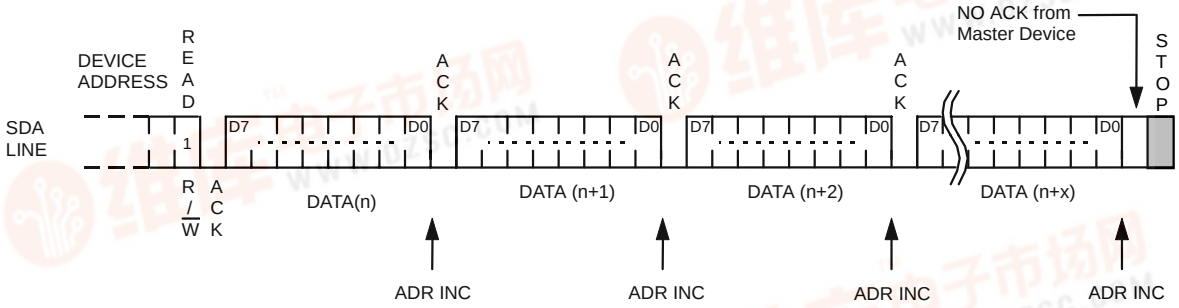


Figure 17 Sequential Read

8. Address increment timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the falling edge of the SCL clock for the 8th bit of the received data in write operation.

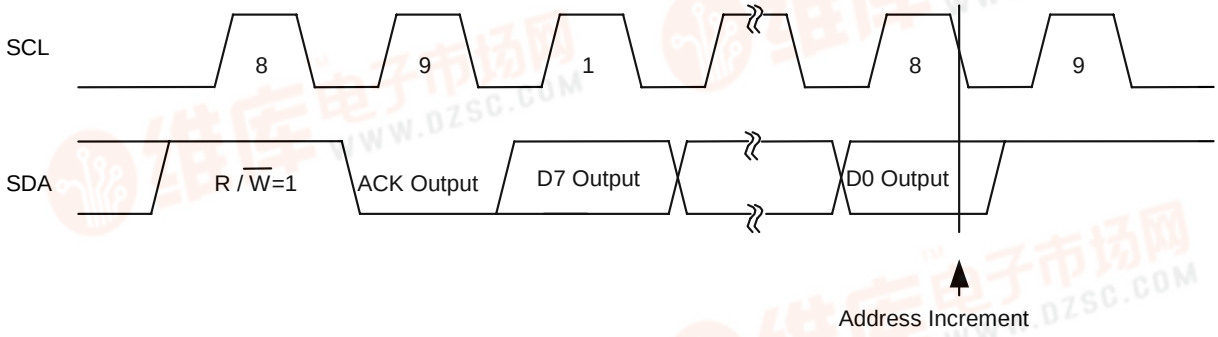


Figure 18 Address Increment Timing in Reading

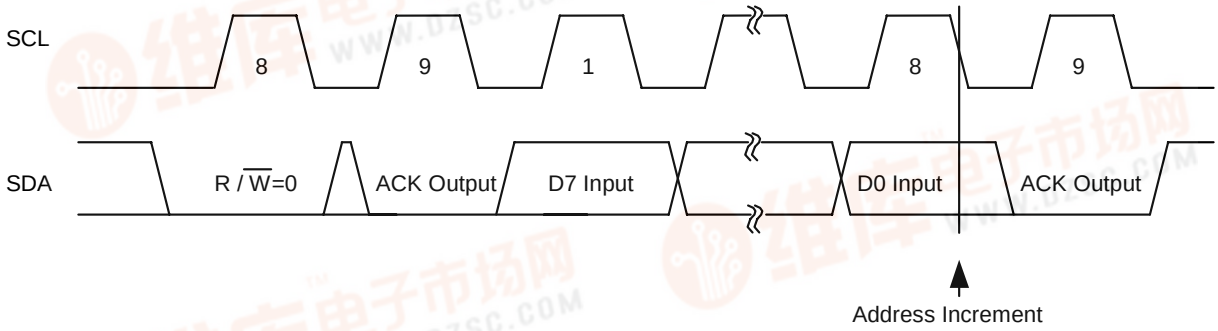


Figure 19 Address Increment Timing in Writing

■ Write Protect Function during the Low Power Supply Voltage

The S-24CS01A/02A/04A has a detection circuit for low power voltage. The detection circuit cancels a write instruction when the power voltage is low or the power switch is on. The detection voltage is 1.75 V typically and the release voltage is 2.05 V typically, the hysteresis of approximate 0.3 V thus exists. (See **Figure 20**.)
When a low power voltage is detected, a write instruction is canceled at the reception of a stop condition.
When the power voltage lowers during a data transmission or a write operation, the data at the address of the operation is not assured.

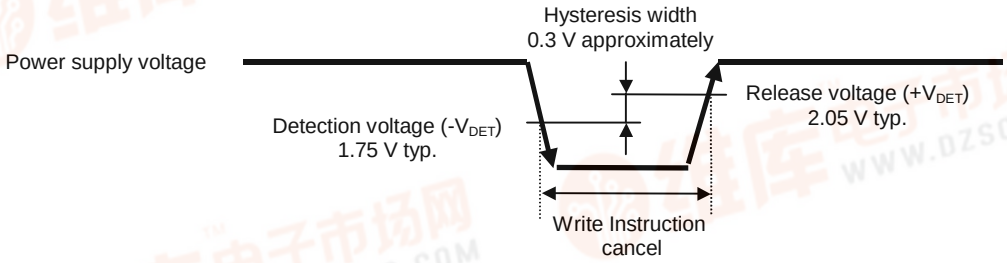


Figure 20 Operation during Low Power Supply Voltage

■ Using S-24CS01A/02A/04A

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 kΩ to 5 kΩ pull-up resistor to the SCL input pin*1 and the SDA I/O pin in order to enable the functions of the I²C-bus protocol. Normal communication cannot be provided without a pull-up resistor.

***1.** When the SCL input pin of the S-24CS01A/02A/04A is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin. This protects the S-24CS01A/02A/04A from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. Equivalent circuit of input and I/O pin

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

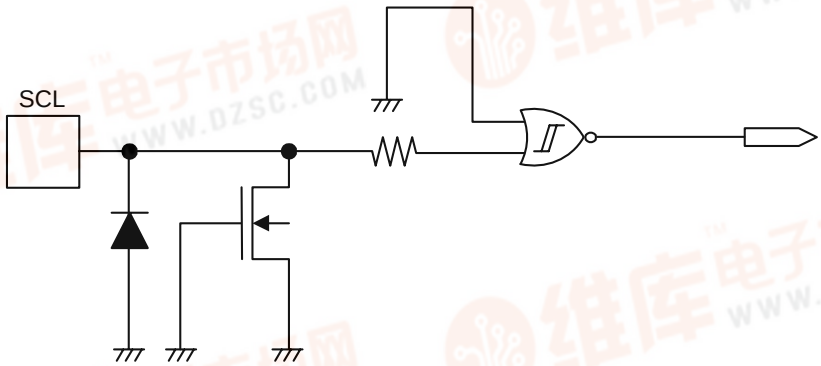


Figure 21 SCL Pin

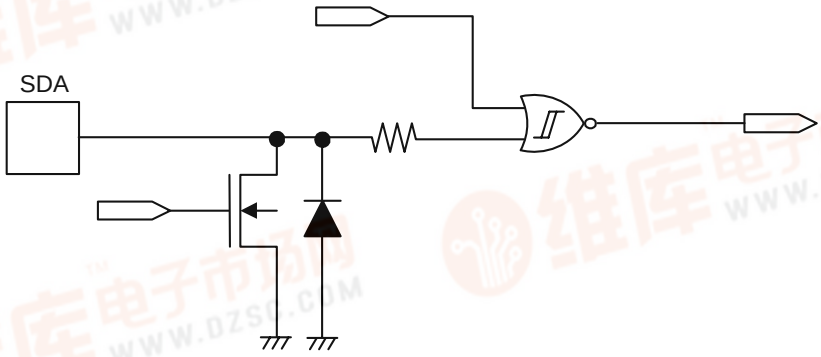


Figure 22 SDA Pin

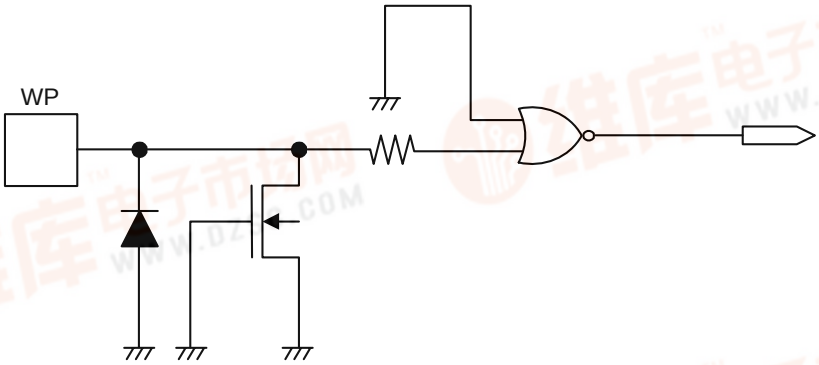


Figure 23 WP Pin

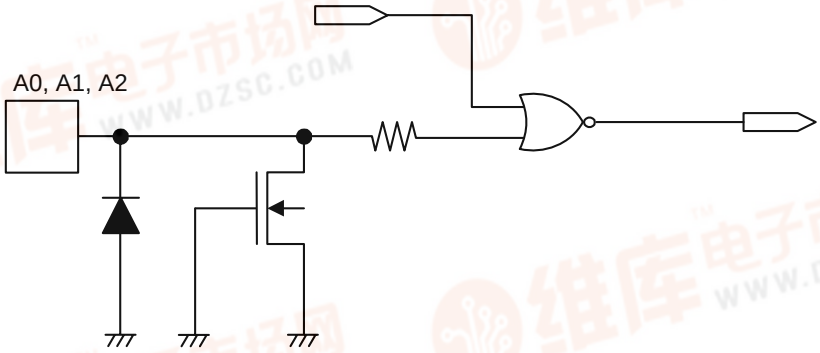


Figure 24 A0, A1, A2 Pin

3. Matching phases while S-24CS01A/02A/04A is accessed

The S-24CS01A/02A/04A does not have a pin for resetting (the internal circuit), therefore, the S-24CS01A/02A/04A cannot be forcibly reset externally. If a communication interruption occurs in the S-24CS01A/02A/04A, it must be reset by software.
For example, even if a reset signal is input to the microprocessor, the internal circuit of the S-24CS01A/02A/04A is not reset as long as the stop condition is not input to the S-24CS01A/02A/04A. In other words, the S-24CS01A/02A/04A retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the S-24CS01A/02A/04A (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset S-24CS01A/02A/04A]

The S-24CS01A/02A/04A can be reset by the start and stop instructions. When the S-24CS01A/02A/04A is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 25** shows this procedure.
First, input the start condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the S-24CS01A/02A/04A interrupts the acknowledge output operation or data output, so input the start condition*1. When a start condition is input, the S-24CS01A/02A/04A is reset. To make doubly sure, input the stop condition to the S-24CS01A/02A/04A. Normal operation is then possible.

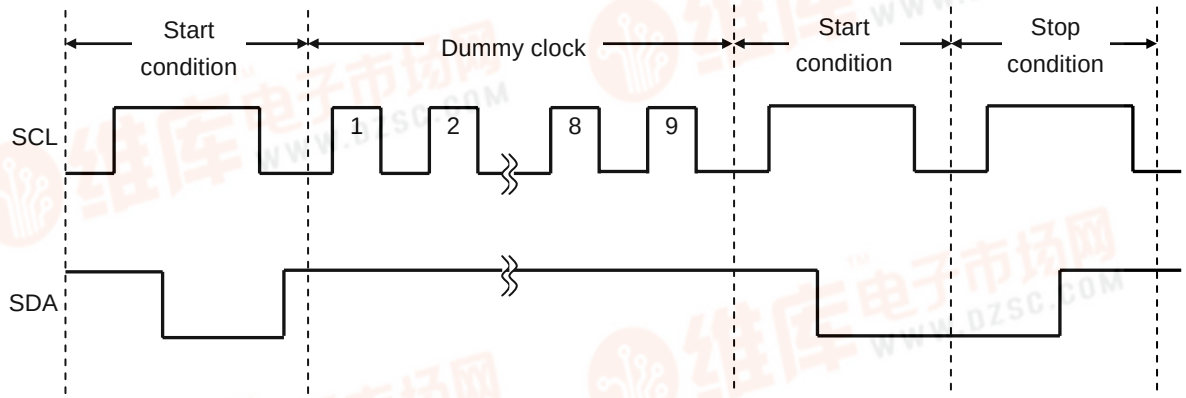


Figure 25 Resetting S-24CS01A/02A/04A

***1.** After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

4. Acknowledge check

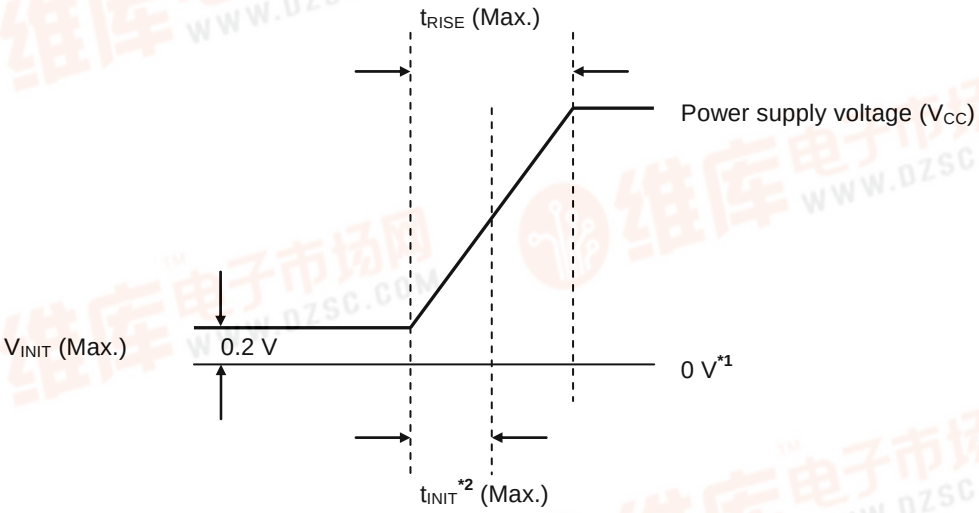
The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and S-24CS01A/02A/04A. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

5. Built-in power-on-clear circuit

S-24CS01A/02A/04A has a built-in power-on-clear circuit that initializes the S-24CS01A/02A/04A. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

5. 1 Raising power supply voltage

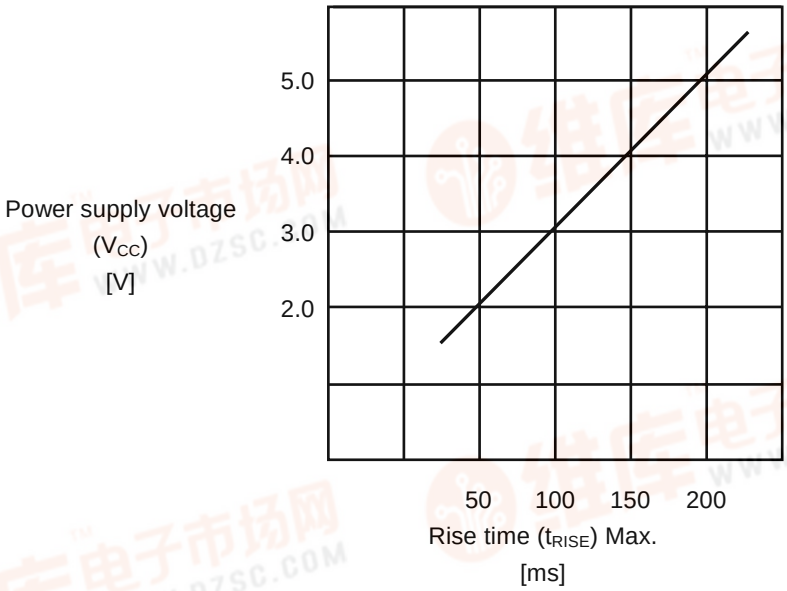
Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 26**.
For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in **Figure 27**. The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the VCC pin and the GND pin of the S-24CS01A/02A/04A.

***2.** t_{INIT} is the time required to initialize the S-24CS01A/02A/04A. No instructions are accepted during this time.

Figure 26 Raising Power Supply Voltage



For example:

If your E²PROM supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 27 Raising Time of Power Supply Voltage

When initialization is successfully completed via the power-on-clear circuit, the S-24CS01A/02A/04A enters the standby status.

If the power-on-clear circuit does not operate, the following are the possible causes.

(1) Because the S-24CS01A/02A/04A has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
(2) The voltage may have dropped due to power off while the S-24CS01A/02A/04A is being accessed. Even if the microprocessor is reset due to the low power voltage, the S-24CS01A/02A/04A may malfunction unless the power-on-clear operation conditions of S-24CS01A/02A/04A are satisfied. For the power-on-clear operation conditions of S-24CS01A/02A/04A, refer to **5. 1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal S-24CS01A/02A/04A circuit is normally reset. The statuses of the S-24CS01A/02A/04A immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

5. 2 Wait for the initialization sequence to end

The S-24CS01A/02A/04A executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 28**.

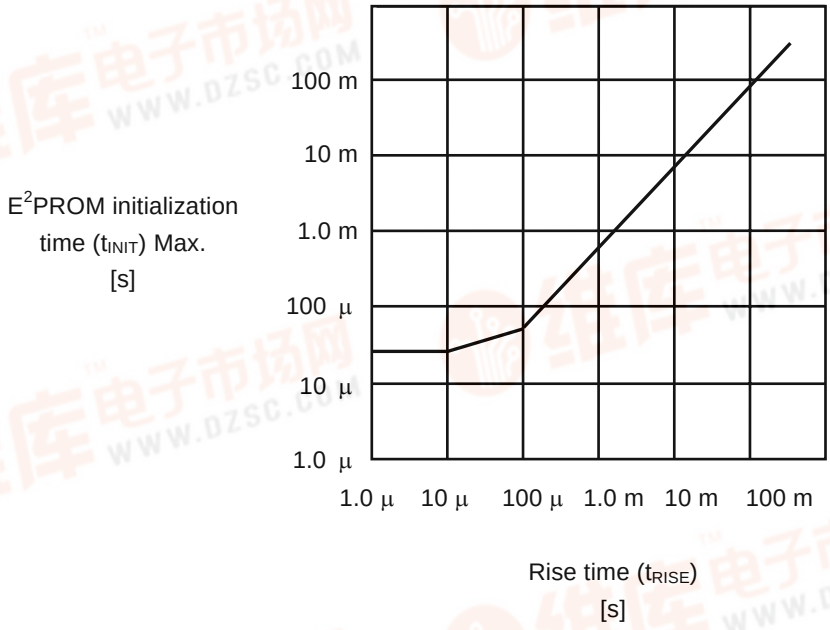


Figure 28 Initialization Time of S-24CS01A/02A/04A

6. Data hold time ($t_{HD.DAT}$ = 0 ns)

If SCL and SDA of the S-24CS01A/02A/04A are changed at the same time, it is necessary to prevent the start/stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the S-24CS01A/02A/04A enters the standby status.
It is recommended that SDA is delayed from the falling edge of SCL by 0.3 μs minimum in the S-24CS01A/02A/04A. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.

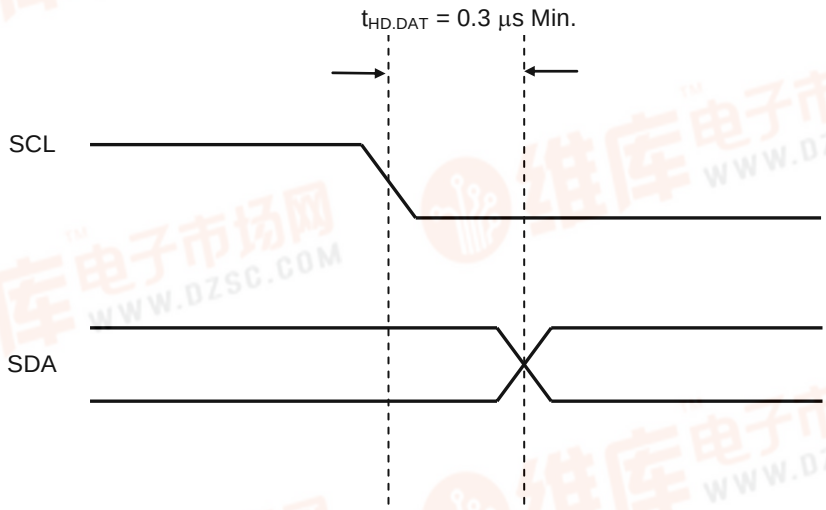


Figure 29 S-24CS01A/02A/04A Data Hold Time

7. SDA pin and SCL pin noise suppression time

The S-24CS01A/02A/04A includes a built-in low-pass filter to suppress noise at the SDA and SCL pins. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 160 ns or less can be suppressed.
The guaranteed for details, refer to noise suppression time (t_I) in **Table 12**.

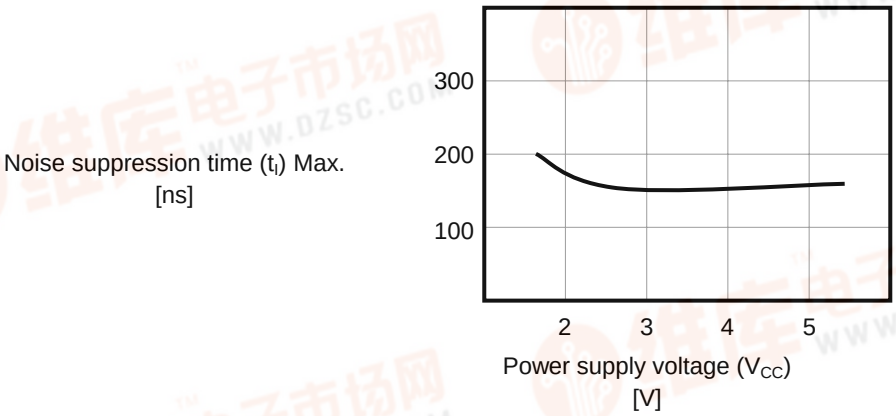


Figure 30 Noise Suppression Time for SDA and SCL Pins

8. S-24CS01A/02A/04A operation in case that the stop condition is received during write operation before receiving the defined data value (less than 8-bit) to SCL pin

When the S-24CS01A/02A/04A receives the stop condition signal compulsorily, during receiving 1 byte of write data, "write" operation is aborted.
When the S-24CS01A/02A/04A receives the stop condition signal after receiving 1 byte or more of data for "page write", 8-bit of data received normally before receiving the stop condition signal can be written.

9. S-24CS01A/02A/04A operation and write data in case that write data is input more than defined page size at "page write"

When write data is input more than defined page size at page write operation, for example, S-24CS04A (which can be executed 16-byte page write) is received data more than 17 byte, 8-bit data of the 17th byte is over written to the first byte in the same page. Data over the capacity of page address cannot be written.

10. Severe environments

Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

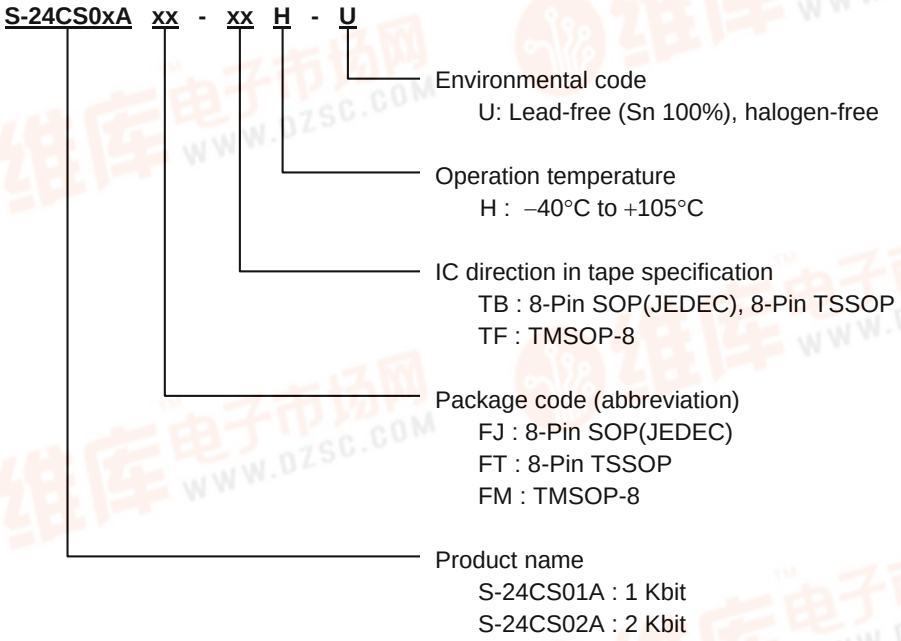
Operations with moisture on the S-24CS01A/02A/04A pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the S-24CS01A/02A/04A up from low temperature tank during the evaluation. Be sure that not remain frost on S-24CS01A/02A/04A pin to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

■ Precaution

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protect circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Product Name Structure

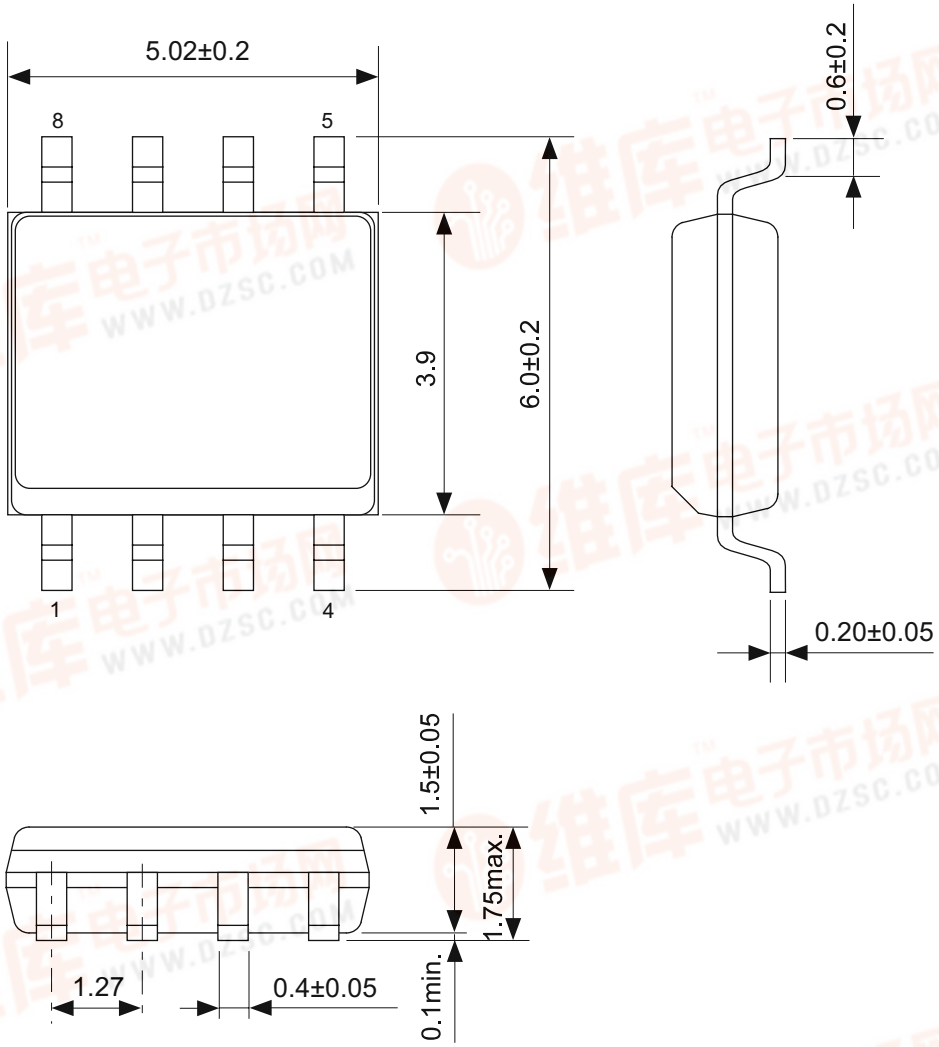
1. Product Name



Remark Please contact our sales office for products with product name structure other than those specified above.

2. Package

Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP(JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-S1
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD



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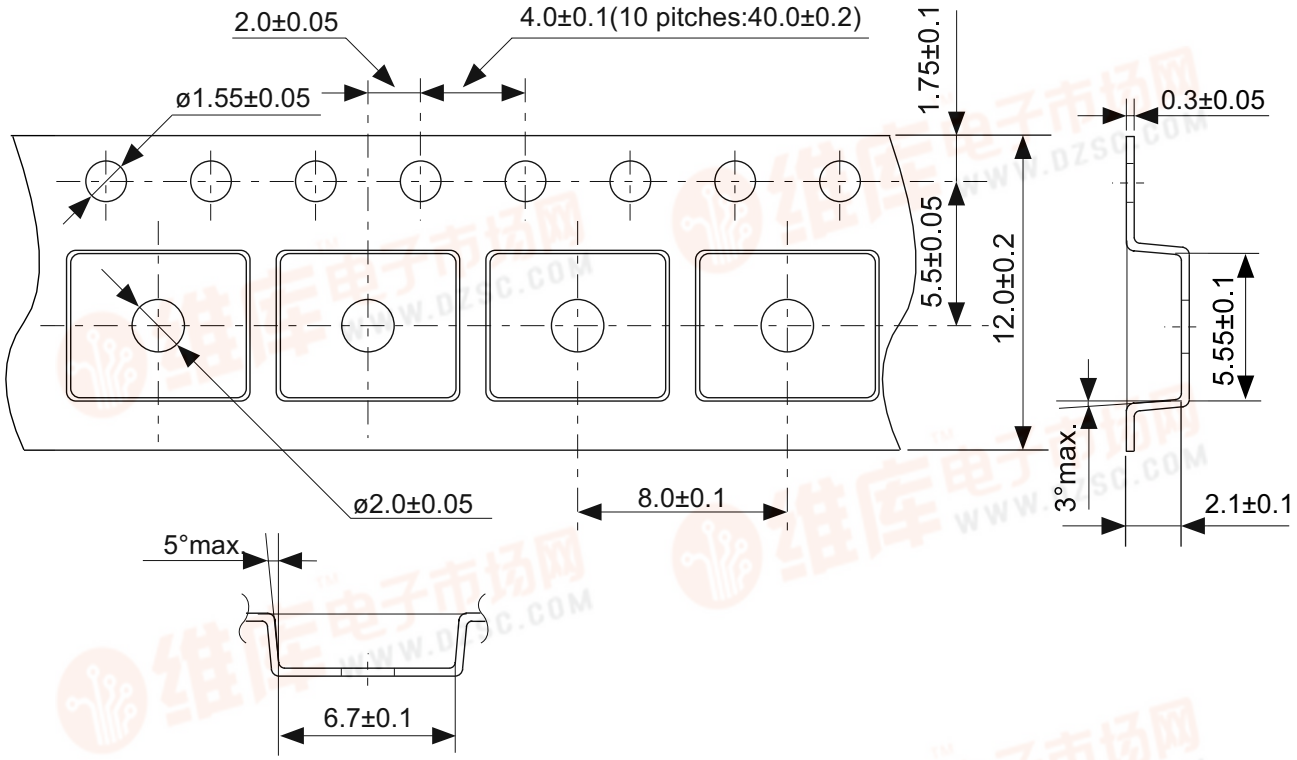
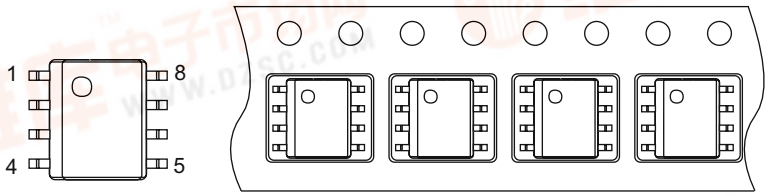
UNIT	mm
Seiko Instruments Inc.	





Feed direction

No. FJ008-D-C-SD-1.1

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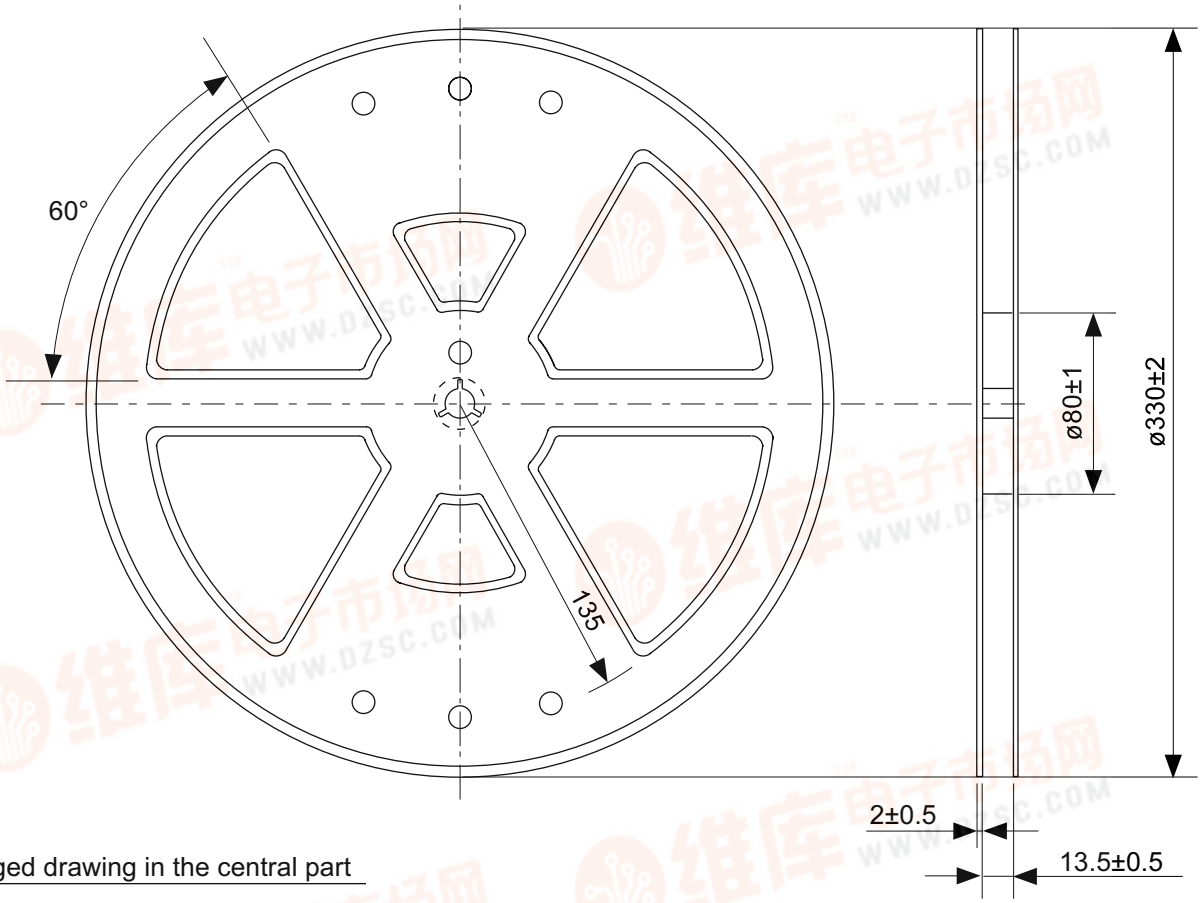
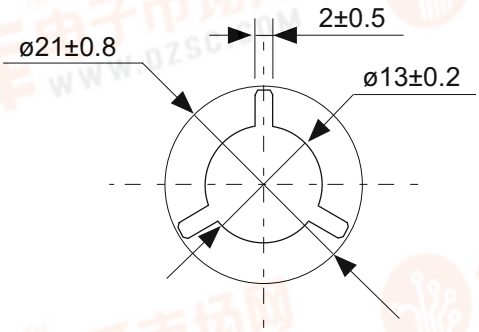
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



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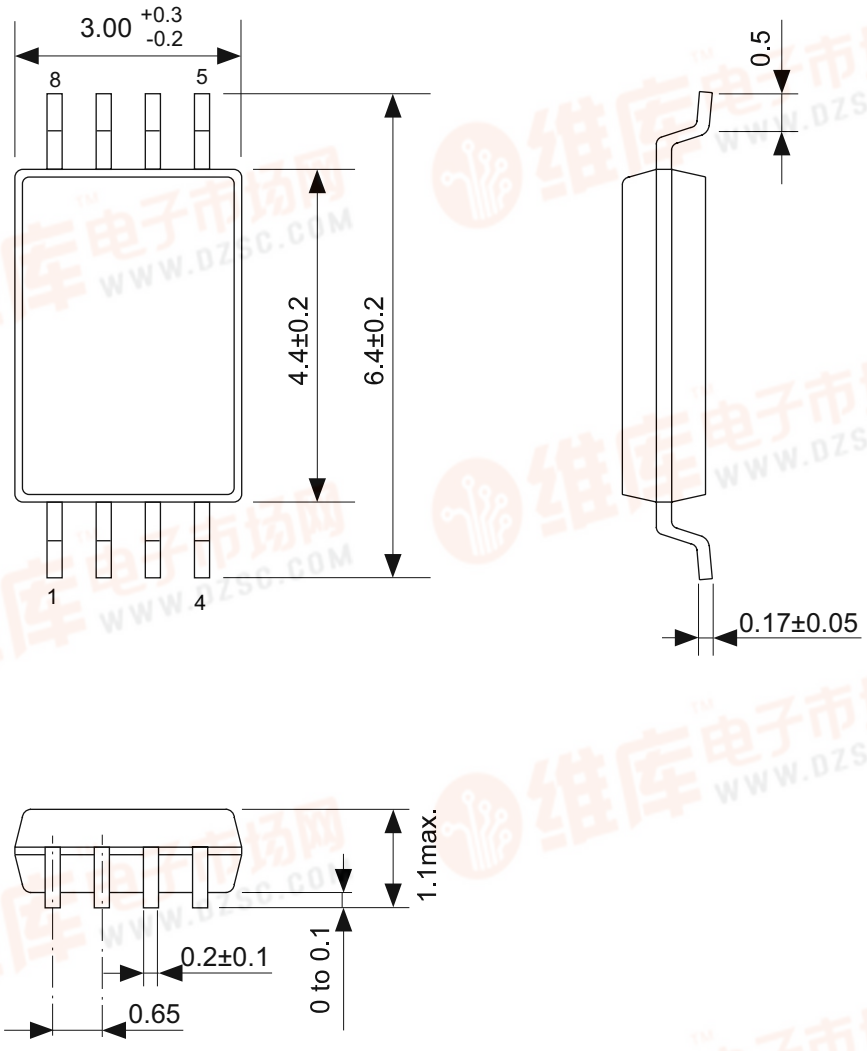
Seiko Instruments Inc.			



No. FT008-A-P-SD-1.1

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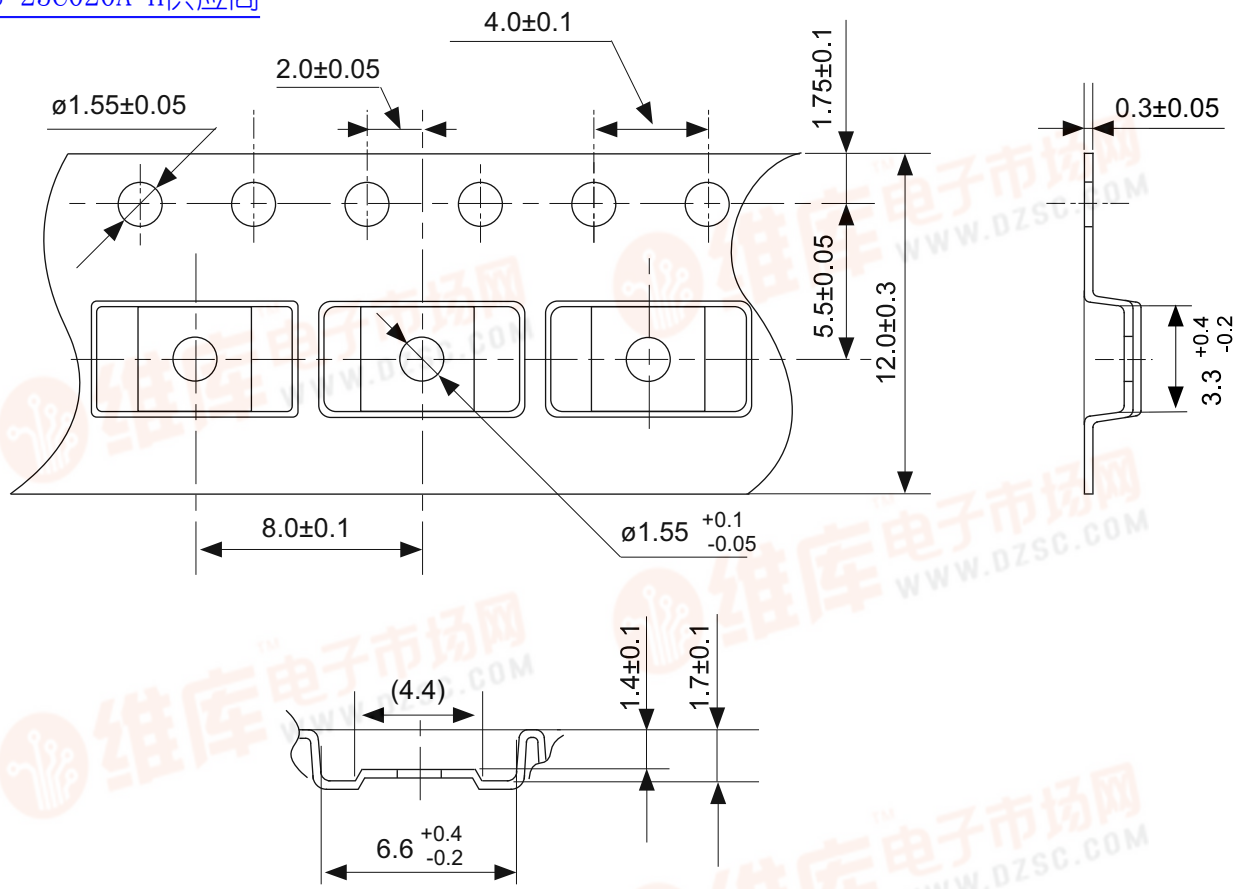
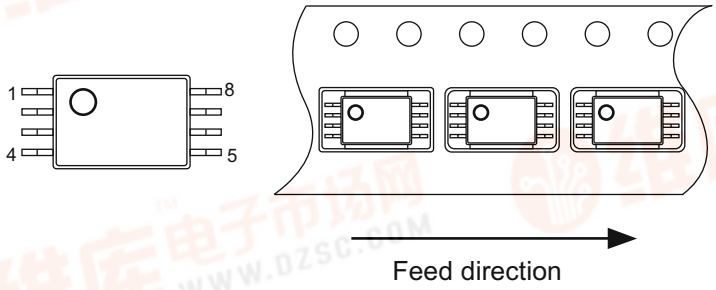
UNIT	mm
Seiko Instruments Inc.	





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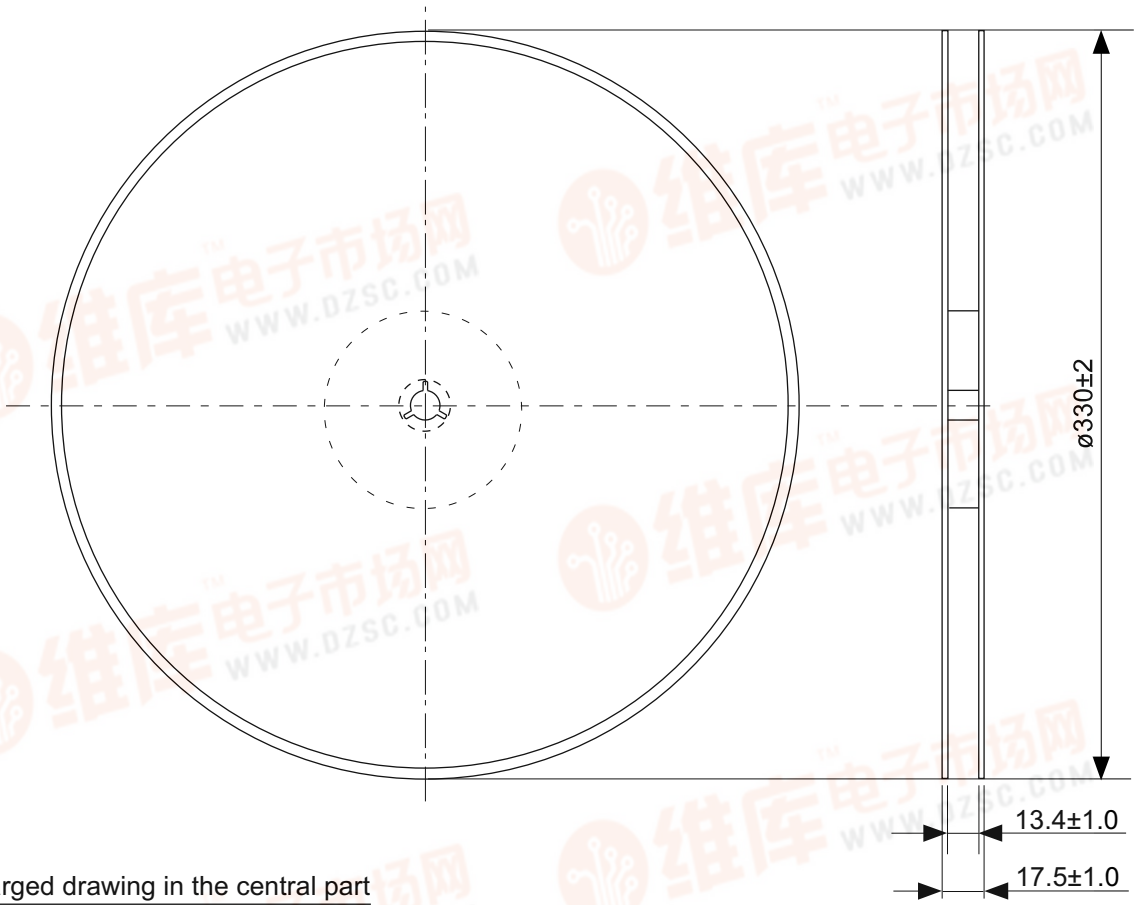
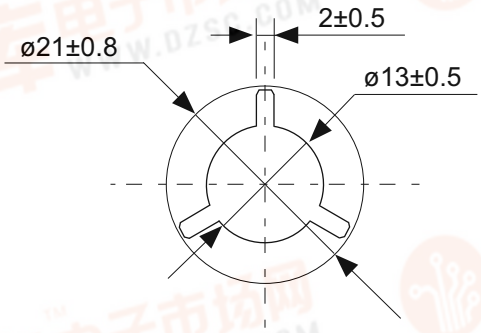
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

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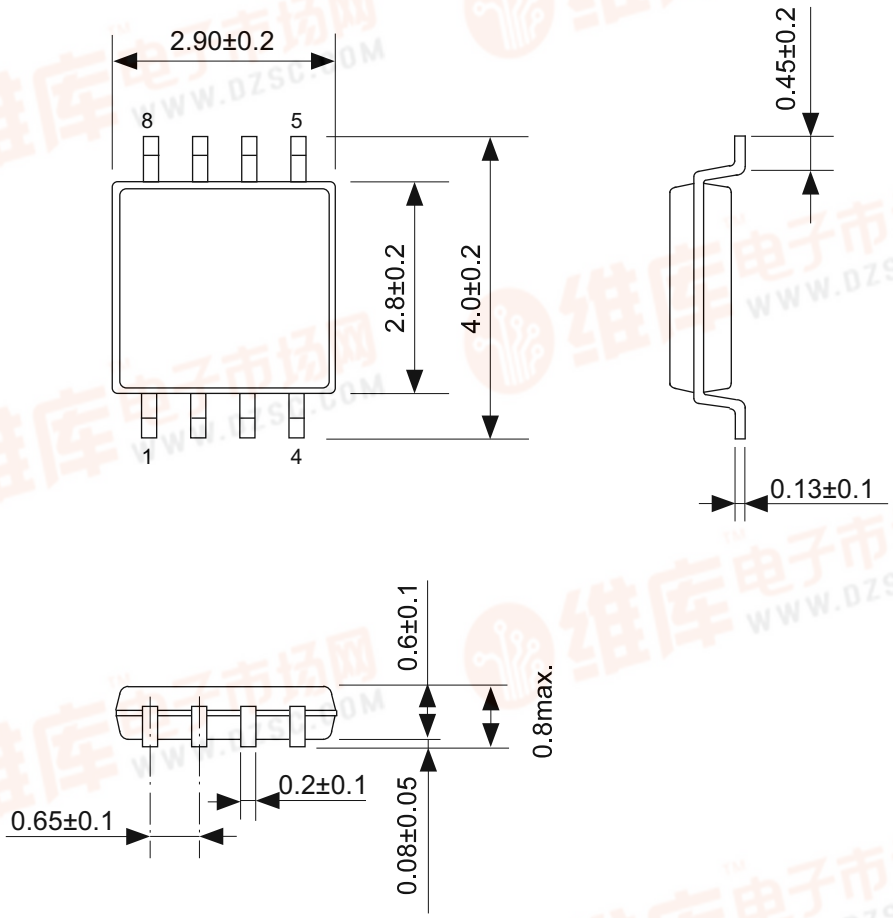
UNIT	mm		
Seiko Instruments Inc.			



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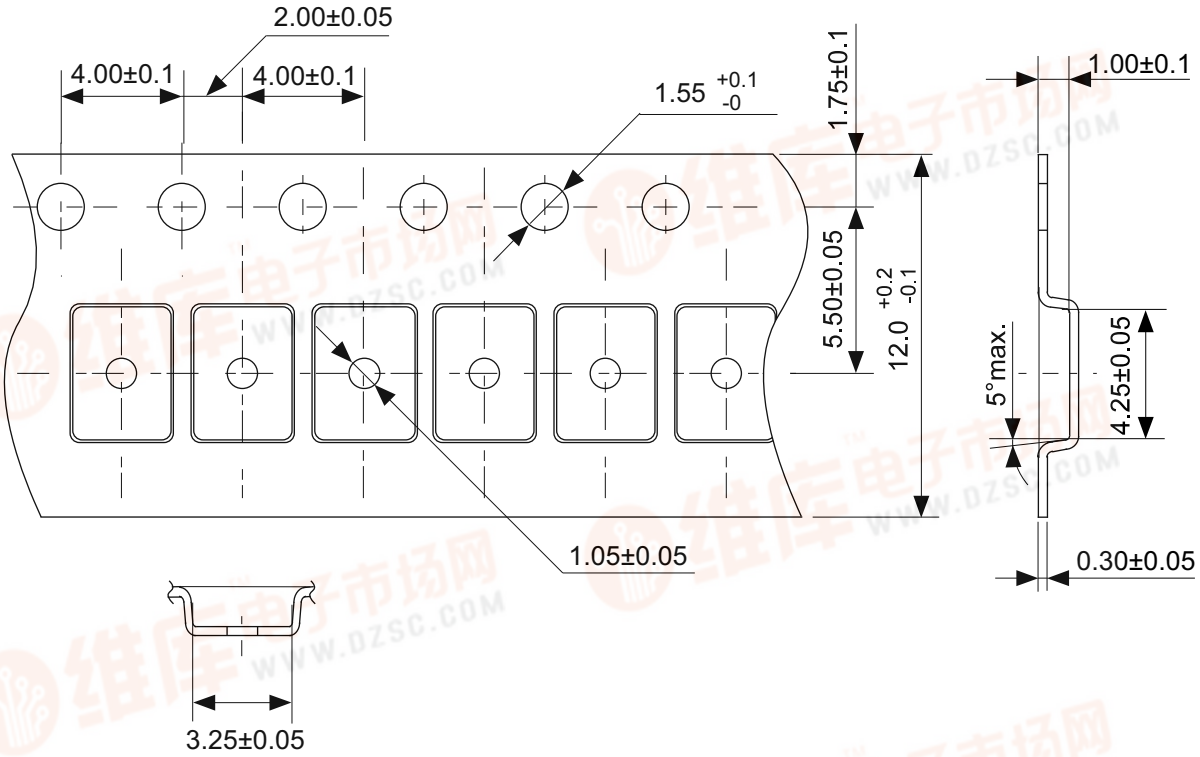
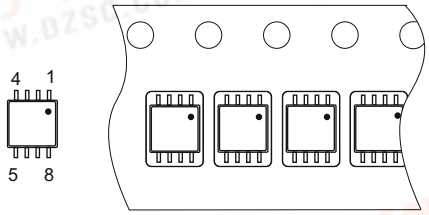
Seiko Instruments Inc.	

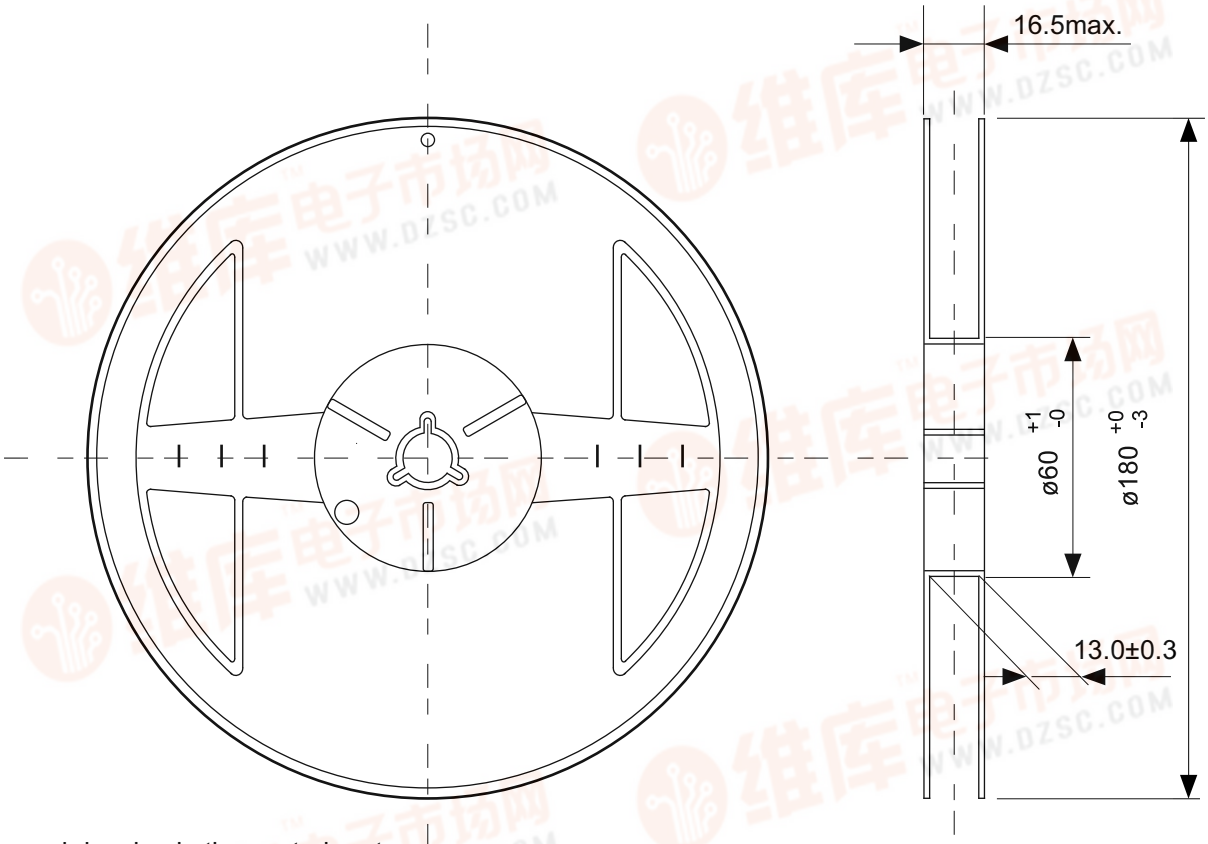




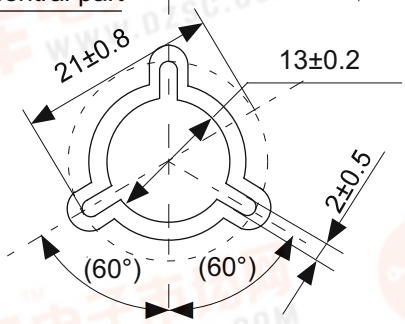
Feed direction

No. FM008-A-C-SD-1.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
SCALE		QTY.	4,000
UNIT	mm		
Seiko Instruments Inc.			

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